IN THE SPECIFICATION:

Please replace the paragraph beginning at page 5, line 22, with the following rewritten paragraph:

Figure **1** schematically illustrates an exemplary configuration for a program execution control system according to the present invention. The system shown in Figure **1** is used for controlling the execution of a program in an information processor of the type processing instructions by pipelining. As shown in Figure **1**, the system includes instruction providing section **10**, instruction executing section **20** and nullification controller **30**. The instruction providing section **10** includes program counter **11**, memory **12** and instruction register **13**. The program counter **11** sequentially specifies respective addresses of instructions to be fetched and executed. The memory **12** reads out the instructions, which together constitute a program (i.e., instruction set) including an execution control instruction, one after another in accordance with the addresses specified. And the instruction register **13** stores thereon the instructions read out one by one. An instruction set **INST** is provided from the instruction register **13** to the instruction executing section **20** and to the nullification controller **30**. The instruction executing section **20** includes: an arithmetic logic unit (ALU) **21** for performing arithmetic or logic operations in response to the instruction set **INST** provided; and a flag register **22** for holding multiple flags indicating the results of the computations. The nullification controller **30** receives control flags **CF** from the flag register **22**. In the illustrated embodiment, the control flags **CF** include two flags **F1** and **F2**, which have been set equal to zero or one by the ALU **21**.

Please replace the paragraph beginning at page 6, line 24, with the following rewritten paragraph:

Figure **2** illustrates a basic format for an execution control instruction according to the present invention. As shown in Figure **2**, the execution control instruction contains instruction field **41**, condition field **42** and instruction-specifying field **43**. The instruction field **41** specifies the type of the instruction as an execution control instruction. The condition field **42** specifies an execution condition **EC**. And the instruction-specifying field **43** defines, in binary code, the number **N** (where N is a natural number) of instructions that will be executed only conditionally, i.e., just when the execution condition **EC** is satisfied. In response to the execution control instruction, the nullification controller **30** decides based on the control flags **CF** whether or not the execution condition **EC** specified by the condition field **42** is met. And based on the outcome of this decision, the nullification controller **30** determines whether or not the number **N** of instructions, which number has been defined by the instruction-specifying field **43** [for] <u>as the number of</u> instructions succeeding the execution control instruction, should be nullified. Suppose the nullification controller **30** has determined that the number **N** of instructions should be nullified since the execution condition **EC** is not met, the controller **30** asserts a nullification signal **NUL** to be supplied to the ALU **21**. In that case, even if the number **N** of instructions following the execution control instruction have already been executed to a midway point of the pipeline, these instructions are nullified in the ALU **21**. Accordingly, the same results are attained as if NOP (no